Please amend the claims as indicated below:

1. (Amended) A hardware emulator for verifying a plurality of systems on a plurality of chips, said emulator comprising:

a first circuitry for verifying a first system on a chip; and

a second circuitry for verifying a second system on another chip while verifying the first system on chip.

2. (Original) The hardware emulator of claim 1, further comprising:

a first interface for providing inputs to the first circuitry and receiving outputs from the first circuitry; and

a second interface for providing inputs to the second circuitry and receiving outputs from the second circuitry.

3. (Amended) The hardware emulator of claim 1, wherein the first circuitry is configured to realize the first system on a chip and the second circuitry is configured to realize the second system on another chip.

4. (Amended) A hardware emulator for verifying a plurality of systems on a plurality of chips, said emulator comprising:

a first circuitry configured to realize a first system on a chip; and

a second circuitry configured to realize a second system on another chip while verifying the first system on chip, the second circuitry connected to the first circuitry.

5. (Original) The hardware emulator of claim 4, further comprising:

a first interface operably connected to the first circuitry, wherein the first interface provides inputs to the first circuitry and receives outputs from the first circuitry; and

a second interface operably connected to the second circuitry, wherein the second interface provides inputs to the second circuitry and receives outputs from the second circuitry.

6. (Original) A method for verifying a plurality of systems on chip, the method comprising:

verifying a first system on a chip with a first portion of a hardware emulator; [and]

verifying a second system on another chip with a second portion of the hardware emulator while verifying the first system on chip;

configuring the first portion of the hardware emulator to realize the first system on chip; and

configuring the second portion of the hardware emulator to realize the second system on chip.

Claim 7 is cancelled without prejudice.

8. (Amended) The method of claim [7] 6, wherein configuring the first portion of the hardware emulator comprises receiving a portion of a top wrapper describing the first system on chip and wherein configuring the second portion of the hardware emulator comprises receiving another portion of a top wrapper describing the second system on another chip.

9. (Original) The method of claim 6, wherein verifying the first system on chip further comprises:

providing inputs to the first portion; and receiving outputs from the first portion.

10. (Amended) A computer readable medium for configuring a hardware emulator, said computer readable medium storing a top wrapper [for configuring a hardware emulator, the top wrapper] comprising:

a first design structure for describing a first system on chip; and

a second design structure for describing a second system on another chip.

11. (Amended) A computer readable medium for configuring a hardware emulator, said computer readable medium storing a data structure, the data structure comprising:

a first design structure for describing a first system on chip, wherein the first design structure further comprises:

a first ports declaration for describing ports associated with the first system on chip;

a first design information for describing at least a portion of the first system on chip; and

an end of first design structure indicator, for indicating the end of the first design structure; and

a second design structure for describing the second system on chip, wherein the second design structure further comprises:

a second ports declaration for describing ports associated with the second system on another chip;

a second design information for describing at least a portion of the first system on another chip; and

an end of second design structure indicator, for indicating the end of the second design indicator; and

the second design structure immediately following the end of first design structure indicator.